AMENDMENTS TO THE CLAIMS

1-8. (Canceled).

9. (Currently Amended) A data sharing apparatus comprising:

a data bus having a data width;

a memory;

a first-endian processor logically connected to said memory in a first-endian byte order via said data bus;

a second-endian processor logically connected to said memory in the first-endian byte order via said data bus; and

an address conversion unit operable:

(i) to invert values of two least significant bits of an address outputted from said second-endian processor and output an address including the inverted values to said memory when said second-endian processor performs a memory access for 8-bit data;

(ii) to invert a value of a second least significant bit of an address outputted from said second-endian processor and output an address including the inverted value to said memory when said second-endian processor performs a memory access for 16-bit data; and

(iii) to output an address from said second-endian processor to the memory without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus, wherein said memory stores structure data to be accessed by said first-endian processor and said second-endian processor,

wherein the structure data includes first structure data and second structure data,

said first-endian processor executes a first program ~~that defines~~ including the first structure data in which data is defined to be in a defined order,

said second-endian processor executes a second program ~~that defines~~ including the second structure data in which ~~includes~~ data that is smaller than the basic word ~~length, the data being~~ length is defined ~~in an~~ to be in an order ~~within the basic word length, and the order being in reverse to an~~ that is reverse of the defined order in the first ~~program~~structure data, and

said first-endian processor reads or writes the structure data to communicate with said second-endian processor, and said second-endian processor reads or writes the structure data to communicate with said first-endian processor.

10. (Previously Presented) The data sharing apparatus according to Claim 9, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

11. (Previously Presented) The data sharing apparatus according to Claim 10,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.

12-15. (Canceled).

16. (Currently Amended) A data sharing apparatus comprising:

a data bus having a data width;

a memory;

a first-endian processor logically connected to said memory in a first-endian byte order via said data bus;

a second-endian processor logically connected to said memory in the first-endian byte order via said data bus; and

an address conversion unit operable:

(i) to invert values of two least significant bits of an address outputted from said second-endian processor and output an address including the inverted values to said memory when said

second-endian processor performs a memory access for 8-bit data;

(ii) to invert a value of a second least significant bit of an address outputted from said second-endian processor and output an address including the inverted value to said memory when said second-endian processor performs a memory access for 16-bit data; and

(iii) to output an address from said second-endian processor to the memory without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus,

wherein the structure data includes first structure data and second structure data,

a cache memory logically connected to the data bus in a second-endian byte order

wherein said memory stores structure data to be accessed by said first-endian processor and said second-endian processor,

said first-endian processor executes a first program ~~that defines~~ including the first structure data in which data is defined to be in a defined order, and

said second-endian processor executes a second program ~~that defines~~ including the second structure data in which ~~includes~~ data that is smaller than the basic word ~~length, said data being~~ length is defined ~~in an~~ to be in an order ~~within the basic word length, and said order being in reverse to an~~ that is reverse of the defined order in the first ~~program~~structure data, and

said first-endian processor reads or writes the structure data to communicate with said second-endian processor, and said second-endian processor reads or writes the structure data to communicate with said first-endian processor.

17. (Previously Presented) The data sharing apparatus according to Claim 16, further comprising a transfer unit operable to control data transfer by direct memory access,

wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.

18. (Previously Presented) The data sharing apparatus according to Claim 17,

wherein the transfer unit includes a conversion unit operable to convert at least one lower bit

of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus, and output the converted address to the memory, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.

19. (Currently Amended) A method of sharing data in a data processing apparatus which includes a first-endian type processor and a second-endian type processor, and a memory to which both processors are connected via a data bus in a first-endian byte order and which stores structure data to be accessed by said first-endian processor and said second-endian processor, the structure data including first structure data and second structure data, the method comprising:

causing the first processor to execute a program ~~that defines~~ including the first structure data in which data is defined to be in a defined order, causing the second processor to execute a program ~~that defines~~ including the second structure data in which ~~includes~~ data that is smaller than a basic word ~~length, said structure data being shared in the memory, said data being~~ length is defined ~~in an~~ to be in an order ~~within the basic word length, and said order being in reverse to an~~ that is reverse of the defined order in ~~a definition of said~~ the first structure data ~~for the first-endian type processor~~, causing the first-endian processor to read or write the structure data to communicate with the second-endian processor, and causing the second-endian processor to read or write the structure data to communicate with the first-endian processor;

(i) inverting values of two least significant bits of an address outputted from the second-endian processor and outputting an address including the inverted values to the memory when the second-endian processor performs a memory access for 8-bit data;

(ii) inverting a value of a second least significant bit of an address outputted from the second-endian processor and outputting an address including the inverted value to the memory when the second-endian processor performs a memory access for 16-bit data; and

(iii) outputting an address from the second-endian processor to the memory without address conversion when the second-endian processor performs a memory access for data having the width of the first data bus.

20-23. (Canceled).

24. (Previously Presented) The data sharing apparatus according to claim 16, wherein the first-endian type is big-endian and the second-endian type is little-endian.

25. (Previously Presented) The data sharing apparatus according to claim 16, wherein the first-endian type is little-endian and the second-endian type is big-endian.

26. (Previously Presented) The method according to claim 19, wherein the first-endian type is big-endian and the second-endian type is little-endian.

27. (Previously Presented) The method according to claim 19, wherein the first-endian type is little-endian and the second-endian type is big-endian.

28-31 (Canceled).